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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/875,364	06/05/2001	Jung-Bae Lee	9898-173	7447

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/875,364	LEE ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-21 and 29* is/are allowed.

6)☒ Claim(s) *1-11,13-15 and 22-28* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The Amendment filed on 08/09/2005 has been entered. Claims 1-29 are pending in this Office action.

Response to Arguments

2. Applicant's arguments, see page 13 under Remarks, filed on 08/09/2005, with respect to the rejection(s) of claim(s) 1-5,13,23,24 and 26 under 35 U.S.C 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hase et al. U.S. Patent 5,636,254.

3. The objection of claim 22 has been withdrawn after Applicants correct the informalities.

Claim Objections

4. Claim 4 is objected to because of the following informalities: in line 2, "the controllable delay unit" should be changed to -- the control unit --. Appropriate correction is required.

5. Claim 5 is objected to because of the following informalities: in line 1, "the controllable delay unit" should be changed to -- the control unit --. Appropriate correction is required.

6. Claim 5 is objected to because of the following informalities: in line 1, "the controlling unit" should be changed to -- the control unit --. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-11, 13-15, 22-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hase et al. U.S. Patent 5,636,254.

Regarding claim 1, figure 2 illustrates an embodiment of an acquisition circuit including a window adjustment circuit 1 includes a delay line 2 to be controlled in an analog fashion and a delay PLL 3 for controlling the delay line 2; see column 4, lines 25-50. Figure 8 shows details of the PLL 3.

Referring back to figure 2, the acquisition circuit includes a first signal transmission path for receiving a reference signal, which is delayed by the first delay time.

The acquisition circuit further comprises a read data path, which corresponds to the claimed second signal transmission path and is delayed by a second delay line from the read data path.

Referring to figure 8, in column 7, lines 4-40, the reference signal 7 is fed to an analog variable delay 55, the reference signal 7 corresponding to the claimed auxiliary signal transmission path.

The analog variable delay 55 corresponds to the claimed master delay unit for generating a master output signal.

Hase et al. does not expressly disclose a control unit as set forth in the application claim. However, as disclosed in figure 8, Hase et al. further teaches that the PLL 3 compares reference signal 7 with control signal 12 to generate an adjustment control 12. In view of that, because phase comparator 51, charge pump 52, V/I 54 generates an adjustment control signal responsive to the reference signal 7 and output from the analog variable delay 55, one of person of ordinary skill in the art would have recognized the interchangeability of phase comparator 51, charge pump 52, V/I 54, taught in Hase et al. invention, for the control unit claimed by Applicants.

Referring back to figure 2, the delay line 2, corresponding to the claimed slave delay unit, for generating a second output signal responsive to the control signal 12.

Regarding claim 2, in column 2, lines 54-67, Hase et al. discloses that the variable delay circuit of the first delay means is supervised according to a stable external reference signal such that the amount of delay matched a delay time decided by the external reference. The variable delay circuit of the second delay means delaying a signal as an object of processing is supervised according to the delay amount control signal obtained from the first delay means. In view of the foregoing teachings, the reference signal 7, corresponding to the claimed auxiliary transmission path, is closely a replica of the read data path.

Regarding claim 3, as recited in claim 2, see also figure 8, the variable delay circuit of the first delay means is supervised according to a stable external reference signal such that the amount of delay matched a delay time decided by the external reference. The variable delay circuit of the second delay means delaying a signal as an object of processing is supervised according to the delay amount control signal obtained from the first delay means. In light of the foregoing, the control signal 12 is adjusted such that the delayed reference signal 7 substantially equals to delay read data signal plus any internal delay time.

Regarding claim 4, delay PLL 3 inherently includes a voltage-controlled delay, see figure 8.

Regarding claim 5, in column 7 line 55 via column 8 line 30, figure 11 shows another embodiment in which the signal processing is applied to a write compensation circuit of a data write circuit. According to the aforementioned embodiment, the selector 151 receives a plurality of delay branches and selects one of the delay branches, responsive to the delay signal B 159. In this embodiment, selector 151 and analog variable N-tap delay 150 constitutes the claimed controllable delay unit.

Regarding claim 6, claim 6 is rejected on the same ground as for claim 1 because of similar scope. Furthermore, the delay PLL 3 corresponds to the claimed controlling unit and the delay line 2 would correspond to the claimed controllable delay unit.

Regarding claim 7, referring to figures 2 and 8, because the delay line 2, corresponding to the claimed controllable delay unit, is controlled in analog fashion (see column 4, lines 29-35), it would have been obvious for one of ordinary skill in the art at the time of the invention that the delay line 2 can be modified to implement as an analog variable delay, which is similar to the analog variable delay 55 in the PLL 3 of figure 8. The motivation for the implementation is modularity of components. The PLL 3 produces a control signal 12 to match the delay of the analog variable delay 55 to the internal delay of the delay line 2.

Regarding claim 8, claim 8 is rejected on the same ground as for claim 5 because of similar scope.

Regarding claim 9, the PLL 3 includes a phase detector 51 performing the claimed limitations.

Regarding claim 10, claim 10 is rejected on the same ground as for claim 5 because of similar scope.

Regarding claim 11, referring to figure 8, the PLL further includes a charge pump 52 for generating an error signal. In the embodiment of figure 7, Hase et al. teaches the analog variable delay 49 is a ring oscillator and in another embodiment of figure 9, the synchronous read clock is a voltage, which controls the delay of delay line 2 in figure 2. In light of the teachings in various embodiment, one of ordinary skill in the art would have been motivated to implement the delay line 2 and the analog variable delay 55 as voltage controlled variable delay units as claimed by Applicants.

Regarding claim 13, claim 13 is rejected on the same ground as for claim 9 because of similar scope.

Regarding claim 14, claim 14 is rejected on the same ground as for claim 6 in view of claim 9 because of similar scope. Furthermore, in column 2, lines 10-25, Hase et al. further discloses that the signal processing delay circuit constituting a stable high-

precision switch adjustment circuit including a delay circuit having an amount of delay invariable with respect to non-uniformity in quality of the manufactured circuit chip, alteration in power, and change in temperature. And in column 2, lines 50-67, the first analog variable delay circuit of the *first delay means is supervised according to a stable external reference signal such that the amount of delay thereof matches a delay time decided by the external reference signal*. The delay amount control operation is desirably carried out through a closed loop control operation, which leads to a highly accurate control operation independent of the variation in quality of the circuit chip, deviation in power, and change in temperature. The amount of delay of the second analog variable delay circuit of the second delay means delaying a signal as an object of processing is supervised according to the delay amount control signal obtained from the first delay means. In light of the foregoing, the first delay means is adjusted according to the fixed delay amount determined by the external reference signal. Therefore, the control signal 12 is adjusted in accordance to the fixed delay amount determined by the external reference signal. As result of that, the voltage level of the control signal 12 is proportional to the phase difference according to a constant due to the fixed delay amount determined by the external reference signal. Because the first delay means (analog variable delay 55 in figure 4) is supervised according to a stable external reference, output of the first delay means is compared with the phase of the reference signal, therefore, the internal phase delay has a magnitude proportional to the voltage level of the control signal 12 according to another proportional constant.

Regarding claim 15, because the external reference signal determines the fixed delay amount, the proportionality constants are selectable as appreciated by one of ordinary skill in the art. Therefore, the product of the first and second proportionality constants can be fixed to certain values including the claimed limitation.

Regarding claim 22, claim 22 is rejected on the same ground as for claim 9 because of similar scope.

Regarding claim 23, claim 23 is rejected on the same ground as for claim 6 because of similar scope.

Regarding claim 24, claim 24 is rejected on the same ground as for claim 3 because of similar scope.

Regarding claim 25, claim 25 is rejected on the same ground as for claim 1 and further in view of claim 3 because of similar scope.

Regarding claim 26, claim 26 is rejected on the same ground as for claim 9 because of similar scope.

Regarding claim 27, claim 27 is rejected on the same ground as for claim 6 because of similar scope.

Regarding claim 28, claim 28 is rejected on the same ground as for claim 11 and further in view of claim 3 because of similar scope.

Allowable Subject Matter

8. Claims 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claim 16 is allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 16, claim 16 is allowed over prior art of record since the cited references, taken individually or in combination, do not teach a signal transmission circuit comprising "wherein the controlling unit comprises: a plurality of delay elements. each of which delays the first temporary signal by a predetermined delay time and outputs a delayed output signal; phase detectors corresponding the plurality of delay elements, each of the phase detectors for outputting phase comparison signals by comparing the phase of one signalof the output signals of the delay elements with the phase of the first signal transmission path and an encoder for receiving each of the phase comparison signals output from the phase detectors and generating the control code".

10. Claims 17-21 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 17, claim 17 is allowed over prior art of record since the cited references, taken individually or in combination, do not disclose a data latch circuit as set forth in the application claim.

11. Claim 29 is allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 29, claim 29 is allowed over prior art of record since the cited references, taken individually or in combination, do not disclose a signal transmission circuit comprising a controlling unit and a second digital code controlled variable delay unit as set forth in the application claim.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh Cong Tran 10/14/2005

Examiner KHANH TRAN